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(71) Applicant
STC plc (United Kingdom),
190 Strand, London WC2R 1DU

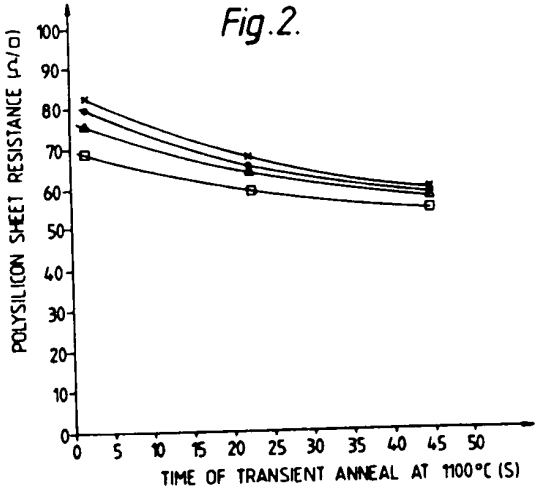
(72) Inventors
Peter Denis Scovell
Roger Leslie Baker

(74) Agent and/or Address for Service
J P W Ryan,
STC Patents, Edinburgh Way, Harlow, Essex CM20 2SH

(54) Polysilicon conductive layers integrated circuits

(57) Low resistivity doped polysilicon conductive layers are formed on an integrated circuit by low temperature recrystallisation of doped amorphous silicon followed by transient pulse annealing to a peak temperature of 1000 to 1100°C to activate the dopant. The pulse annealing effects a reduction in the resistivity compared with previous methods.

Fig.2.



× EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 5'N_2,15'WET O_2,10'N_2 AT 900°C.
∘ EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 5'N_2,15'WET O_2,15'N_2 AT 900°C
△ EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 5'N_2,15'WET $O_2$25'N_2 AT 900°C
□ EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 30'WET O_2, AT 900°C

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Fig.1.

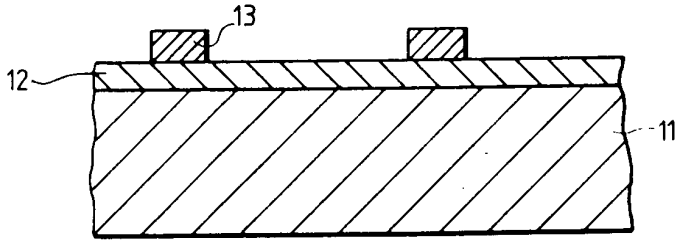
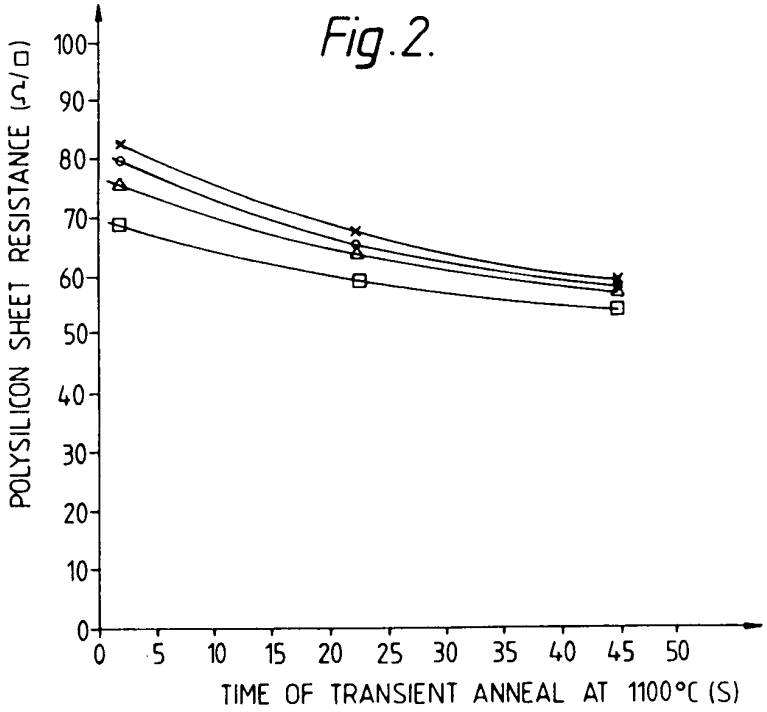


Fig.2.



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△ EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 5'N_2,15'WET $O_2$25'N_2 AT 900°C
□ EXPERIMENTAL RESULT WITH PRELIMINARY DRIVE-IN OF 30'WET O_2, AT 900°C

SPECIFICATION

Improvements in integrated circuits

This invention relates to integrated circuits, and in particular to the provision of polysilicon conductors on such circuits.

Polycrystalline silicon, or polysilicon, is frequently used in the fabrication of conductive regions, e.g. gates and interconnection tracks, on integrated circuits. Its use, particularly in high frequency applications, is however limited by the relatively high resistivity of the material. Attempts have been made to overcome this problem by doping the polysilicon typically with phosphorus, arsenic or boron. It is then necessary to anneal the material to diffuse the dopant thereby achieving the desired low resistivity.

It has been found that, using conventional furnace annealing techniques, much of the dopant is trapped in the grain boundaries of the polysilicon and is therefore inactive. Furthermore, during the annealing process, redistribution of the dopants in underlying active areas can occur. This is clearly particularly undesirable when the circuit comprises small devices at a high integration density.

The object of the present invention is to minimise or to overcome this disadvantage.

According to one aspect of the invention there is provided a process for forming a doped polysilicon pattern on an integrated circuit, the process including providing the doped pattern on the circuit, and pulse heating the assembly to a temperature at which redistribution of the dopant in the polysilicon is effected whereby the resistivity of the doped polysilicon is reduced.

According to another aspect of the invention there is provided a process for forming a doped polysilicon conductive layer on an integrated circuit, the process including providing a doped amorphous silicon layer on said circuit, annealing the circuit at a temperature of 500 to 900°C for a sufficient time to recrystallise the amorphous silicon to form doped polysilicon, and pulse heating the circuit to 1000 to 1110°C thereby activating the dopant whereby the resistivity of the polysilicon is reduced.

As the high temperature excursion requires only a short period of time the risk of dopant redistribution in the circuit is substantially eliminated.

An embodiment of the invention will now be described with reference to the accompanying drawings in which

Figure 1 is a cross-sectional view of an integrated circuit provided with a silicon conductor pattern, and

Figure 2 illustrates the relationship between doped polysilicon sheet resistance and anneal time.

Referring to the Fig. 1, a semiconductor substrate 11 incorporating a plurality of active devices (not shown) is provided with an insulating layer 12 of a refractory material, e.g. silica or silicon nitride. The insulating layer is in turn coated with a patterned layer 13 of doped polycrystalline silicon. Typically the assembly comprises a merged technology circuit in which a number of both CMOS and bipolar devices are provided on a common substrate. The polysilicon layer 13 may thus provide an interconnection pattern, the CMOS gates, and bipolar polysilicon emitters. Such a structure is described in our copending UK application No. 8507624. The resistivity of the polysilicon 13 is reduced by effecting recitivation of the dopant. This is performed by pulse heating the assembly to a temperature at which reactivation occurs. As this thermal treatment is relatively short there is no significant effect on circuit devices formed in the substrate 11.

In a typical process an integrated circuit is provided with a doped polysilicon conductor pattern formed from an amorphous silicon layer. Such a layer may be deposited by LPCVD (low pressure chemical vapour deposition), PECVD (plasma enhanced chemical vapour deposition) or reactive sputtering. The amorphous silicon is doped, e.g. with phosphorus, arsenic or boron. Doping can be effected chemically during growth or subsequently by ion implantation. The assembly is then heated to a temperature of 500 to 1000°C to recrystallise the material to form polysilicon. At the relatively low temperatures employed to effect this recrystallisation substantially no dopant redistribution occurs in the integrated circuit. Typically the dopant comprises 0.3 to 3 At % of the amorphous silicon.

During this recrystallisation of the amorphous silicon most of the dopants are trapped in non-substitutional sites in the growing crystals and are thus electrically inactive. The dopant is fully activated by a short high temperature excursion to e.g. 1000 to 1110°C for 0.5 to 5 seconds in a transient annealing apparatus. We have found that the use of transient annealing to activate the dopants minimises segregation to grain boundaries and thus provides a high dopant activity and a low resistivity. Typically the final resistivity is from 2 to 15 m ohm cm.

Masking and etching of the silicon layer to define the desired conductor pattern may be performed at a convenient stage in the process. Typically, etching is effected after crystallisation but before dopant activation.

In an alternaive process the silicon layer 13 may be deposited as a doped or undoped material in polycrystalline form, thus obviating the recrystallisation step in the process. Where undoped material is used, doping may be effected by ion implantation.

In a typical example we have formed in situ phosphorus doped amorphous silicon films

containing 0.3 At % of dopant. These were found to have a resistivity of 25 m ohm cm. The films were annealed at 850°C for 50 minutes to recrystallise the silicon and then had a measured resistivity of 20 m ohm cm. Pulse annealing of the films for 1 second at 1100°C using incoherent radiation provided a final resistivity of 14 m ohm cm. Similarly treated films containing 2.5 At % phosphorous had a measured resistivity of 6.2 m ohm cm after annealing for 1 second at 1000°C compared wifth 30 m ohm cm prior to recrystallisation.

The relationship between annealing time and sheet resistance is illustrated in Fig. 2 of the accompanying drawings. Measurements have been made on four silicon films each of 4300A (430nm) thickness. In each case the material was implanted with arsenic at 40 keV with a dose of 1.5E16 cm^{-2} followed by a preliminary drive in at 900°C. The final sheet resistances observed correspond to resistivities in the range 2.4 to 3.65 m ohm cm.

The use of transient annealing for dopant activation together with low regrowth temperatures is particularly suited to the low temperature process requirements for advanced CMOS and bipolar circuits. It is not however limited to these particular processes and has general semiconductor application.

CLAIMS

1. A process for forming a doped polysilicon pattern on an integrated circuit, the process including providing the doped pattern on the circuit, and pulse heating the assembly to a temperature at which redistribution of the dopant in the polysilicon is effected whereby the resistivity of the doped polysilicon is reduced.

2. A process for forming a doped polysilicon conductive layer on an integrated circuit, the process including providing a doped amorphous silicon layer on said circuit, annealing the circuit at a temperature of 500 to 900°C for a sufficient time to recrystallise the amorphous silicon to form doped polysilicon, and pulse heating the circuit to 1000 to 1110°C thereby activating the dopant whereby the resistivity of the polysilicon is reduced.

3. A process as claimed in claim 1 or 2, wherein the dopant is phosphorus arsenic or boron.

4. A process as claimed in claim 1, 2 or 3, wherein the dopant comprises 0.3 to 3 At % of the amorphous silicon.

5. A process as claimed in claim 1, 2, 3 or 4, wherein the dopant is introduced by ion implantation into the amorphous silicon layer.

6. A process as claimed in any one of claims 1 to 5, wherein the resistivity of the polysilicon conductive layer is from 2 to 15 m ohm cm.

7. A process as claimed in any one of claims 1 to 6, wherein the circuit is pulse heated for 0.5 to 5 seconds.

8. A process as claimed in any one of claims 1 to 7, wherein said circuit incorporates both CMOS and bipolar devices.

9. A process as claimed in claim 8, wherein the doped polysilicon layer provides the gates of the CMOS devices, the emitters of the bipolar devices and an interconnect pattern.

10. A process for forming a doped polysilicon layer on an integrated circuit, which process is substantially as described herein with reference to and as shown in the accompanying drawings.

11. An integrated circuit fabricated via a process as claimed in any one of claims 1 to 10.

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